[0023] Therefore, according to the semiconductor device and its manufacturing method of the above aspects of the present invention, there is an advantage that reliability of an ohmic electrode in a high humidity environment can be improved while securing sufficient reliability of an ohmic electrode in a high temperature environment.

BRIEF DESCRIPTION OF THE DRAWINGS

[0024] FIG. **1**(A) is a schematic section view showing a configuration of a semiconductor device according to an embodiment of the present invention, also showing its entire configuration.

[0025] FIG. **1**(B) is a schematic section view showing a configuration of a semiconductor device according to an embodiment of the present invention, also showing a portion of a source electrode or a drain electrode in its enlarged view.

[0026] FIG. **2** is a schematic section view showing a configuration of a semiconductor device according to a modification example of an embodiment of the present invention, also showing a part of a source electrode or a drain electrode in its enlarged view.

[0027] FIG. **3**(A) to FIG. **3**(J) are schematic section views for explaining a method for manufacturing a semiconductor device according to an embodiment of the present invention.

[0028] FIG. **4**(A) is a photo instead of a diagram showing an electrode surface of a semiconductor device according to an embodiment of the present invention in its partially enlarged view.

[0029] FIG. **4**(B) is a diagram schematically showing the photo in FIG. **4**(A).

[0030] FIG. **5** is a schematic section view showing a configuration of a conventional semiconductor device.

[0031] FIG. **6**(A) is a photo instead of a diagram showing an electrode surface of a conventional semiconductor device.

[0032] FIG. **6**(B) is a diagram showing a part of FIG. **6**(A) in its enlarged view.

[0033] FIG. **6**(C) and FIG. **6**(D) are diagrams schematically showing the photos in FIG. **6**(A) and FIG. **6**(B), respectively.

[0034] FIG. **7**(A) is a schematic section view showing a configuration of a semiconductor device proposed in the course of development of the present invention, also showing its entire configuration.

[0035] FIG. **7**(B) is a schematic section view showing a configuration of a semiconductor device proposed in the course of development of the present invention, also showing a part of a source electrode or a drain electrode in its enlarged view.

[0036] FIG. **8**(A) is a photo instead of a diagram showing an electrode surface of a semiconductor device proposed in the course of development of the present invention in its partially enlarged view.

[0037] FIG. **8**(B) is a diagram schematically showing the photo in FIG. **8**(A).

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0038] A semiconductor device and manufacturing method thereof according to an embodiment of the present invention are described below with reference to FIG. **1**(A), FIG. **1**(B), FIG. **2**, and FIG. **3**(A) to FIG. **3**(J).

[0039] The semiconductor device (compound semiconductor device) according to the present embodiment is, for example, a gallium nitride based field effect transistor (GaN-FET; here, HEMT; High Electron Mobility Transistor), and has, for example as shown in FIG. **1**(A) and FIG. **1**(B), a structure in which an intentionally undoped GaN electron transit layer **2** (i-GaN layer) **2**, an electron supply layer **3** made of an n-type $Al_xGa_{1-x}N$ ($0 \leqq x \leqq 1$) layer (n-AlGaN layer), and an n-type GaN layer (n-GaN layer) **8** are stacked in order on an SiC (silicon carbide) substrate **11**. By the way, a spacer layer [for example, an intentionally undoped $Al_xGa_{1-x}N$ ($0 \leqq x \leqq 1$) layer (i-AlGaN layer)] may be provided between the electron transit layer **2** and the electron supply layer **3**.

[0040] On the n-type GaN layer (n-GaN layer) **8**, a gate electrode **5** is provided. In other words, the gate electrode **5** is in Schottky contact with the n-GaN layer **8**. On the other hand, on opposite sides of the gate electrode **5**, a source electrode **12** and a drain electrode **13** are provided on the $Al_xGa_{1-x}N$ ($0 \leqq x \leqq 1$) electron supply layer **3** (that is, n-type GaN based semiconductor layer; n-type III-V group nitride compound semiconductor layer). In other words, both the source electrode **12** and the drain electrode **13** are in ohmic contact with the $Al_xGa_{1-x}N$ ($0 \leqq x \leqq 1$) electron supply layer **3**. In FIG. **1**(A), symbol **4** denotes an SiN passivation film.

[0041] In the present embodiment, both the source electrode **12** and the drain electrode **13** are configured so as to have, for example, a Ta/Al/Ta stacked structure in which a tantalum (Ta) layer (first layer) **9**, an aluminum (Al) layer (second layer) **10**, and the tantalum (Ta) layer (third layer) **9** are stacked in order, as shown in FIG. **1**(B).

[0042] In the present embodiment, in order to configure a high power output device for which a high voltage operation is required, an SiC substrate (high resistance substrate, semi-insulating substrate) having a resistivity of 1×10^6 Ω·cm or more is used as the SiC substrate **11**. The substrate is not limited to this and for example, a conductive substrate (low resistance substrate; for example, metal substrate) having a resistivity of 1×10^5 Ω·cm or less may be used.

[0043] The structure of the source electrode **12** and the drain electrode **13** as an ohmic electrode is not limited to this but it is only required to configure so as to have a structure in which a metal layer made of any one material of tantalum (Ta), palladium (Pd), nickel (Ni), and molybdenum (Mo) is stacked on the Ta/Al stacked structure in which the tantalum (Ta) layer **9** and the aluminum (Al) layer **10** are stacked in order.

[0044] For example, as shown in FIG. **2**, it may also be possible to configure both the source electrode **12** and the drain electrode **13** so as to have a Ta/Al/Pd stacked structure in which the tantalum (Ta) layer **9**, the aluminum (Al) layer **10**, and a palladium (Pd) layer **14** are stacked in order. Further, although not shown, it may also be possible to configure both the source electrode **12** and the drain electrode **13** so as to have a Ta/Al/Ni stacked structure in which the tantalum (Ta) layer **9**, the aluminum (Al) layer **10**, and a nickel (Ni) layer are stacked in order, or configure both the source electrode **12** and the drain electrode **13** so as to have a Ta/Al/Mo stacked structure in which the tantalum (Ta) layer **9**, the aluminum (Al) layer **10**, and the molybdenum (Mo) layer are stacked in order. By the way, in FIG. **2**, a part of the source electrode **12** or the drain electrode **13** is shown in its enlarged view.